# Drain Bias Effects on Statistical Variability and Reliability and Related Subthreshold Variability in 20-nm Bulk Planar MOSFETs

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Abstract—Statistical variability and reliability due to random discrete dopants (RDD), gate line edge roughness (LER), metal gate granularity and N/PBIT associated random charge trapping has limited the progressive scaling of bulk planar MOSFETs beyond the 20-nm technology node. In this paper, their impacts on device figures of merit are studied through comprehensive 3-D simulation. It is found that raised drain-bias can exacerbate threshold-voltage fluctuations, mainly due to LER and RDD. Subthreshold slope (SS) variations resulting from each variation source is studied: RDD and LER generate most of the SS variation and are primarily responsible for its skew. Drain induced barrier lowering (DIBL) is examined against each intrinsic variation source, and RDD and LER are found to cause most of the DIBL variability. The correlation of DIBL with threshold-voltage is fully analysed with respect to each source of statistical variability and reliability. Except for LER, all major sources of variability exhibit de-correlation of DIBL against threshold-voltage.

Keywords: DIBL; drain bias; threshold voltage; subthreshold slope; variability

## I. Introduction

The bulk planar MOSFET architecture is approaching its limit. A three-dimensional multi-gate FinFET architecture has been adopted by Intel at the 22 nm node [1], and a fully-depleted SOI MOSFETs have been introduced by ST Microelectronics at the 28 nm node [2]. However, technology considerations and cost still render bulk planar MOSFETs an attractive technology for many markets [3]. All FET architectures, including bulk planar MOSFETs, are subject to unavoidable statistical variability and reliability issues resulting from the discreteness of charge and granularity of matter—issues which have become a critical concern for device scaling and power dissipation, already affecting adversely the SRAM yield [4].

Such variability arises from atomic scale variations between nominally identical devices and causes measurable intrinsic parameter fluctuations and significant differences in the I-V characteristics between even closely paired

nanoscale transistors. Key sources of such variability are: the random number and position of dopants in nanoscale MOSFETs; the rough edges of gate lines due to the granular nature of photoresist on gate patterning; the work function variations between the polycrystalline grains of some metal gate materials after high-temperature thermal processing; random discrete trapped charges occurring due to negative / positive bias temperature instability (N/PBTI) [5].

When characterising statistical variability and reliability the threshold-voltage fluctuation is the primary figure of merit, but device subthreshold behaviour is not fully captured by threshold-voltage alone. Subthreshold slope (SS) and drain-induced barrier lowering (DIBL) are also of great practical importance. For example, the drain-bias has a strong effect on subthreshold electrostatics, and DIBL is an indicator of the drain bias dependence of the short-channel effects. The geometry, body bias and temperature impact on statistical variability for the 20-nm bulk planar technology was presented in [6]. To the best of our knowledge, there are few systematic studies of the impact of the *drain-bias* on the statistical variability and reliability of bulk MOSFETs [6][7][8]. In this paper the impact of drain-bias on bulk MOSFET threshold-voltage and subthreshold variability is studied in detail, taking into account the individual impact of all relevant major statistical variability sources: random discrete dopants (RDD), line edge roughness (LER) and metal gate granularity (MGG), as well as the random interface trapped charges (ITC) responsible for the bias temperature instability degradation.

## II. Simulation Methodology

The testbed n-channel transistor with a physical gate-length of 25 nm is representative for the 20 nm bulk planar technology node. It features a hafnium-based high-$\kappa$ gate dielectric and TiN metal gate with equivalent oxide thickness of 0.85 nm. The complex doping profiles of this device were optimized in [6], in terms of both nominal device performance and variability. A retrograde doping profile reduces the effective channel doping near the interface, which in turn reduces the RDD-induced variability. In addition, super halo doping profiles were adopted to control short-channel effects. The GSS atomistic simulator GARAND is deployed for both the uniform and the atomistic simulations through this study [9]. Its drift-diffusion module features density gradient quantum corrections carefully calibrated against experimental data [8]. The 'uniform' or nominal n-MOSFET achieves a drive current of 1.35 mA/μm and leakage current of approximately 100 nA/μm. The subthreshold slope (SS) is 89 mV/dec at $V_D$ = 0.05 V and the DIBL is approximately 100 mV/V.

Starting from this nominal transistor, the relevant sources of statistical variability and reliability are introduced to generate microscopically different 'atomistic' devices. RDD is typically the dominant statistical variability source in bulk MOSFETs, and has been intensively studied [10]-[12]. In RDD simulations dopants are randomly assigned to locations in the MOSFET based on the nominal local doping concentration using a rejection technique [13]. The effects of LER and

MGG are also studied. The gate line edge in each device is obtained by Fourier synthesis based on a Gaussian autocorrelation function with 30 nm correlation length and root-mean-square amplitude of 1.33 nm (i.e. LER = 4 nm) [14]. The TiN metal gate-first process, introduced at the 32/28 nm technology node, shows low thermal stability [15] with the polycrystalline microstructure of metal formed during high temperature annealing and/or source/drain doping activation. For MGG simulation the metal gate morphology is randomly selected from patterns on a large TEM image, and an average metal grain diameter of 6 nm is assumed. The two dominant TiN metal grain orientations typically have work-function differences of 0.2 V with 0.4/0.6 probability of occurrence [16][17]. In addition, electrons can be trapped randomly at the oxide interface defect sites due to stress—positive bias temperature instability (PBTI). This random interface trapped charge (ITC) is generated based on average trapped charge density corresponding to different stages of BTI degradation, again using a rejection technique [18]. Figure 1 shows the potential and carrier concentration distributions in one 'atomistic' n-MOFET subject to RDD, LER and MGG. The electron density in the channel and source/drain varies considerably across the device; the potential landscape close to interface is colored by the current density magnitude on the top slice. Distinct electron percolation paths are formed between the potential peaks due to random dopants. The individual and combined statistical variability sources are simulated for ensembles of 200 microscopically different transistors, each with channel width 25 nm. The transfer characteristics of these transistors at $V_D$=1V are plotted in Figure 2. The on-current variation is approximately 11%. The standard deviation of the threshold voltage is 75.6 mV and the standard deviation of the logarithm of the leakage current is 0.81, which means that a one sigma shift changes the off current by a factor of 6.5. The large dispersion in the subthreshold region is crucially important when managing mismatch and overall quiescent power.

## III. Drain bias effects on statistical variability and reliability

### A. Threshold voltage fluctuation

The transfer characteristics of the statistical sample of transistors are simulated at different drain-biases. The threshold-voltage is extracted using a constant current criterion. Figure 3 shows the dependence of the threshold-voltage on drain-bias for the 200 microscopically different MOSFETs subject to combined statistical variability sources including RDD, LER and MGG. As the drain bias increases, the average threshold-voltage decreases, as expected. For such devices, the nominal threshold voltage reduction between $V_D$ = 50 mV and $V_D$ = 1.0 V should clearly approach the DIBL value of ~100 mV/V. The maximum threshold-voltage reduction actually reaches 198 mV, and the minimum change of threshold voltage is 53 mV. It should be noted that many of these curves cross, indicating that the variations are due to a mixture of sources.

Figure 4 shows that the average threshold-voltage decreases as a function of drain-bias, for each separate source of variability. The nominal threshold-voltage

without any variability sources is approximately ~6 mV above the LER curve (and 20 mV below the ITC curve). Variability sources typically induce percolation paths which somewhat lowers the threshold-voltage below its nominal value. Aside from the lowest bias point, the average threshold-voltage linearly decreases with drain bias with a slope of approximately 80mV/V. The average threshold-voltage value decrease is practically independent of any variability source, including random interface trapped charges, where the average sheet charge density of $5\times10^{11}$ $cm^{-2}$ shifts the threshold-voltage up by about 20 mV compared to the nominal device.

The standard deviation of the threshold-voltage ($\sigma V_T$) as a function of the drain voltage, does show a marked dependence on variability source, and this is plotted in Figure 5. Overall, the threshold-voltage fluctuation due to combined statistical variability sources increases with the increase in the drain bias. However, the MGG induced threshold-voltage variation is virtually independent of drain bias. The RDD-induced $\sigma V_T$ increases slightly, from 56 mV to 61 mV, as drain bias increases from 0.05 V to 1.0 V. This is due to the effective channel length reduction caused by the lateral electric field enhanced at high drain-bias. The most drain-bias sensitive variability source is LER. The LER induced $\sigma V_T$ increases from 10 mV to 25 mV as $V_D$ is raised from $V_D$ = 0.05 V to $V_D$ = 1.0 V.

To better understand this effect, the distribution of threshold-voltage values due to gate LER is plotted in Figure 6 using a normal probability Q-Q plot in which a Gaussian distribution is a straight line. The LER-induced threshold-voltage distribution is significantly skewed with prolonged tail towards the lower values. This skew is even more prominent, and its spread is larger, at high drain bias. The skew is caused by the threshold-voltage asymmetrical roll-off characteristics at the nominal design point [8]. As clearly shown in Figure 7, the roll-off slopes become large with increasing drain bias.

B. Subthreshold slope variation

Subthreshold slope (SS) is the measure of efficient gate control and its dependence on variability source is important for quiescent current leakage evaluations. The SS is extracted in the subthresholdregion from the ensemble of transfer characteristics at different drain bias points from $V_D$ = 0.05 V to 1.0 V. In addition to the expected broad range of SS values, Figure 8 also shows considerable diversity in response. Some devices show large increases in SS as a function of drain bias—in some cases of several tens of mV difference. Most devices show the expected increase in subthreshold, and a few devices shows a slight decrease in SS. However, the rapid increase in the spread of SS with drain bias is prominent. In addition, the inset histogram of figure 8 shows that the SS distribution is highly skewed, even at low drain bias.

What is the source of this SS skew? TCAD can perform individual statistical simulations for individual variability sources including RDD, MGG, LER and N/PBTI associated ITC, and can therefore provide deeper insight into the SS distributions. Figure 9 shows the Q-Q plots of SS distributions due to each individual source. While in the presence of MGG, SS demonstrates small variations and close to Gaussian

distribution, RDD and LER induced SS variation is larger, and are the source of the skew in the overall distribution. Without interactions from other variability sources, ITC induces negligible SS variation. Increasing drain bias increases the respective SS variation due to each variability source, but does not change the overall form of the contributions. The following conclusions can be reached: SS is sensitive to variations in the device depletion region, and MGG variations primarily affect the region directly below the insulator, therefore their impact on SS is relatively small. In contrast, LER causes variation over the whole depletion region, and RDD can produce dramatic random doping fluctuations throughout the channel, including in the depletion regions—resulting in largest SS variations. In addition, the correlation between threshold voltage and SS is strong, with coefficients of -0.65 and -0.80 at low and high drain bias respectively. This strong coupling between $V_T$ and SS is again primarily the result of the variation sources, RDD and LER. The correlation coefficients are -0.70∼-0.80 and -0.99 respectively for RDD and LER.

## IV. DIBL variability and correlations

### A. DIBL variability

DIBL variability has already been briefly mentioned in section III.A when considering drain bias effects on $V_T$. Here DIBL as an important figure of merit is considered in more details. DIBL variability can significantly affect SRAM stability [19][20], and therefore a detailed understanding of DIBL variability and its relation to threshold-voltage variability has significant industrial implications. We define DIBL as the threshold-voltage difference at low drain bias ($V_D$ = 0.05 V) and at high drain bias (equalling to supply voltage) normalized by drain bias difference. The DIBL variation due to individual variability sources is shown in Figure 10. RDD causes the largest DIBL variation with a standard deviation of 20.4 mV/V. The next in importance is LER followed by MGG. ITC causes relatively little DIBL variation. The above results support the observations in section III.A.

### B. Correlation between $V_T$ and DIBL

The correlation between threshold voltage and DIBL in bulk planar MOSFETs is weak. For example, the correlation coefficient between DIBL and linear threshold-voltage at $V_D$ = 0.05 V is -0.14, and the correlation coefficient between DIBL and saturation threshold-voltage at $V_D$ = 1.0 V is -0.48. Therefore, subthreshold electrostatic variation is not fully captured by threshold-voltage fluctuation data. Figure 11 presents scatter plots showing the correlation between linear threshold-voltage and DIBL extracted between $V_D$ = 1.0 V and 0.05 V for each variability source. Very strong correlation is observed in the case of LER, but almost no correlation is observed for RDD, MGG and ITC. The weak correlation between $V_T$ and DIBL results primarily from random discrete charges.

In order to understand these correlation features, specific ‘atomistic’ devices with extreme DIBL or $V_T$ values are examined more closely (the starred devices of figure 11).

Figure 12 shows four extremal atomistic devices subject to RDD with high/low threshold-voltages and large/small DIBL values. These are simulated at $V_D$ = 0.05 V and $V_G$ = 0.3 V. The electron density distribution contours are plotted, and the potential landscape close to the oxide interface is coloured by current density. In the presence of RDD, ionised acceptors in the channel produce channel barrier potential peaks, with device figures of merit dependant on both acceptor density and location. It is clear that with fewer acceptors in the channel devices will have a lower threshold-voltage—clearly the case in figures 12 (a) and (c). Although the *position* of the dopants in the channel may affect on threshold-voltage, in these examples the effect is minimal. However in figures 12 (a) and (b) the proportion of acceptors at the drain-side is high. As drain bias, and hence the drain side electric field, increases, the effect of these drain-side dopants in providing a barrier to current is constrained, and the overall source drain potential barrier is significantly reduced [6]. Thus the transistors in figures 12 (a) and (b) exhibit high DIBL values.

The effect of high/low work-function (HWF/LWF) metal grains on the local channel potential is similar to that produced by random channel dopants. Therefore MGG results in a $V_T$ and DIBL correlation similar to that resulting from RDD. In Figure 13, it is evident that the regions affected by metal grains with LWF possess lower potential barrier and higher electron density, and turn on earlier than those governed by metal grains with HWF. Similarly when metal grains of HWF are located near the drain, those devices demonstrate large DIBL.

Trapped charges at oxide interface defect states reduce the local current flow because of the induced Coulomb potential at trap sites. Two simulation devices, with low and high DIBL values respectively, are examined in Figure 14 (a) and (b). It is obvious that trapped charges at either the source or drain sides may cause completely different DIBL characteristics. This effect of interface trapped charge is similar to that of random dopants.

Figure 15 shows devices with extremal DIBL and $V_T$, due to LER. Here, as a result of localised channel shortening, devices generally have low threshold-voltage and poor DIBL simultaneously. Therefore threshold-voltage and DIBL are strongly correlated in the presence of random gate-length variations.

These phenomena are summarised by calculating the corresponding correlation coefficients. The drain-bias dependence of the correlation coefficients between linear threshold-voltage and DIBL for the individual and variability sources is illustrated in Figure 16. LER demonstrates consistently strong correlation between threshold-voltage and DIBL with a correlation coefficient of -0.96. In the RDD case threshold-voltage and DIBL are almost uncorrelated with the correlation coefficient of -0.06. For MGG and ITC there are weak correlations. As indicated in Figure 11, RDD contribute most to the magnitude of the DIBL variability, with the next strongest contribution from LER, therefore they together produce the moderate correlation of threshold-voltage and DIBL in 'atomistic' bulk MOSFETs in the presence of combined statistical variability sources. Our results indicate that in ultra-thin body SOI devices or FinFET structures, which have significantly lower

RDD, the $V_T$ - DIBL correlation is likely to be significantly stronger than in bulk devices.

## V. Conclusions

The drain bias dependence of statistical variability and reliability, especially of threshold-voltage fluctuations and subthreshold variability, has been studied in realistic bulk MOSFETs of 20 nm node. It was found that the threshold-voltage variation increases with increasing drain bias, and LER induced variability shows the largest drain bias dependence, with RDD the next most important contributor of drain-bias dependence. Subthreshold slope variation, and the important skew of its distribution, is caused primarily by RDD and LER. DIBL was shown to have weak correlation with threshold-voltage, but the correlation depends significantly on the variability sources present. LER results in strong correlation between DIBL and the linear threshold-voltage while RDD results in almost complete decorrelation.

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Illustrations

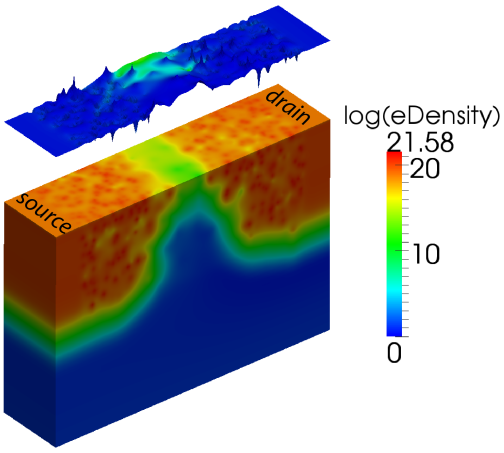


Figure 1. An 'atomistic' n-channel MOSFET, $W=L_G=25nm$, showing the electron density in the simulation domain due to statistical variability sources including RDD, LER and MGG. The top slice shows the potential landscape which is colored by current density magnitude.

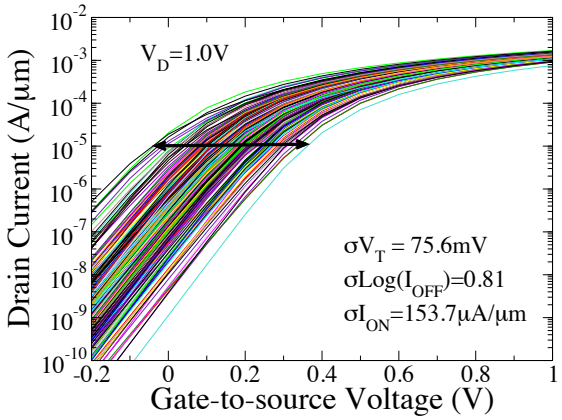


Figure 2. The drain-currrent vs. gate-voltage transfer characteristics of 200 microscopically different nMOSFETs subject to combined statistical variability sources including RDD, LER and MGG.

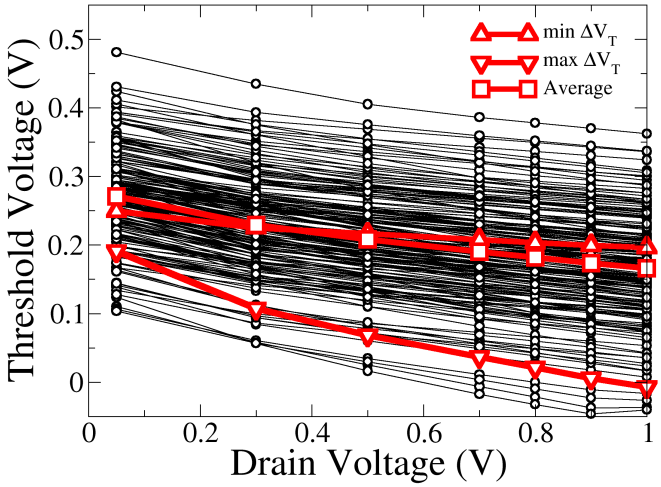


Figure 3. Threshold-voltage at different drain bias for 200 microscopically different nMOSFETs subject to combined statistical variability sources.

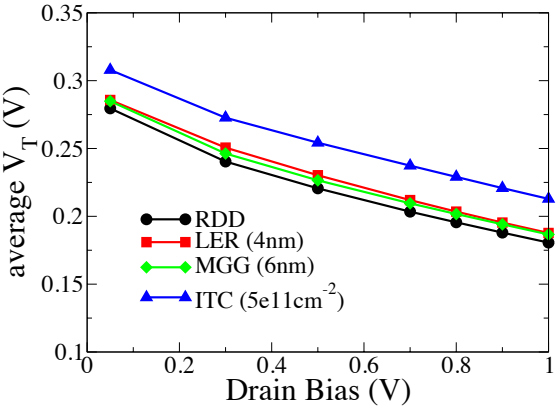


Figure 4. The dependence of average threshold-voltage on drain bias.

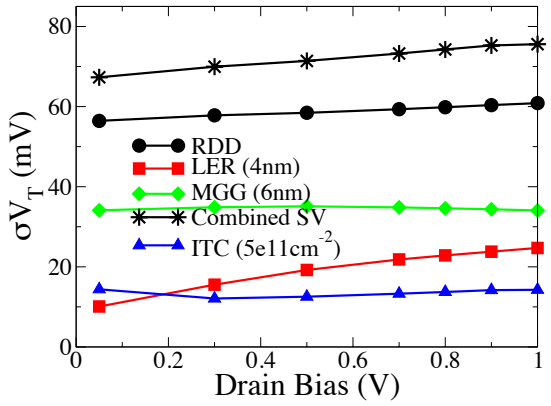


Figure 5. The dependence of standard deviations of threshold-voltages on the drain bias.

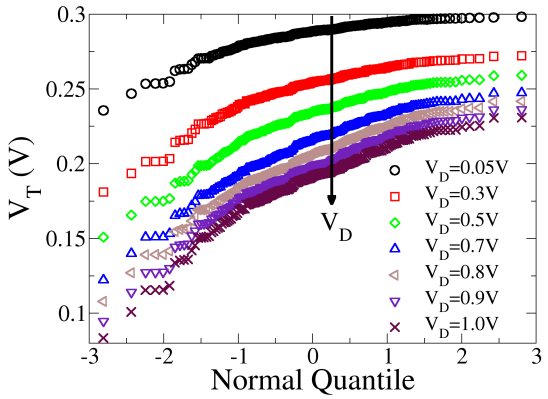


Figure 6. The normal Q-Q plots for threshold voltages due to gate LER at different drain bias.

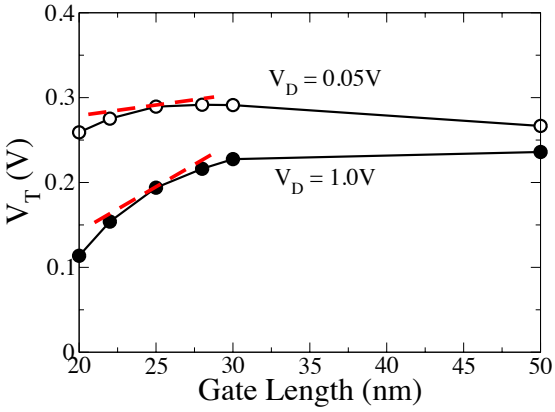


Figure 7. The threshold-voltage roll-off characteristics of uniform nMOSFET at different drain biases.

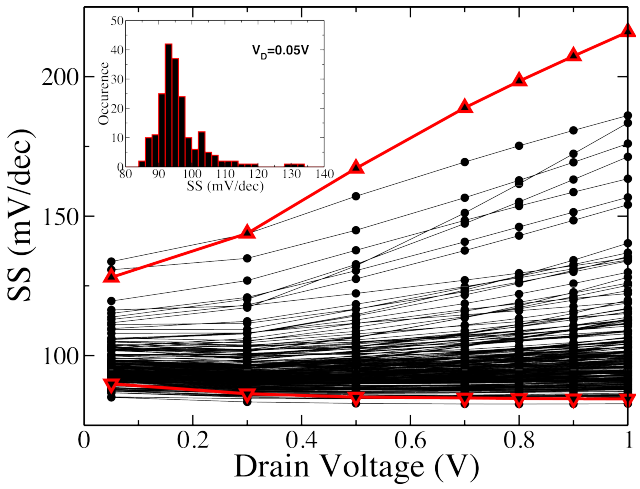


Figure 8. The subthreshold slope extracted from atomistic devices at different drain biases.

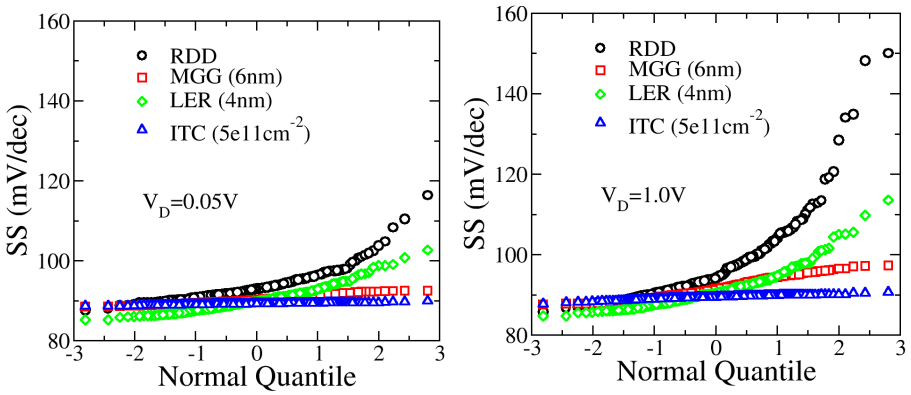


Figure 9. The subthreshold slope QQ plots subject to various sources of statistical variability and reliability.

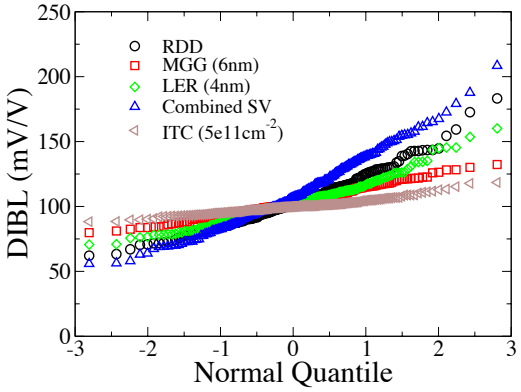


Figure 10. The Q-Q plot of DIBL distributions due to different variability sources. The DIBL is calculated from $V_T$ difference at $V_D$=0.05V and 1.0V, normalized by the drain bias difference.

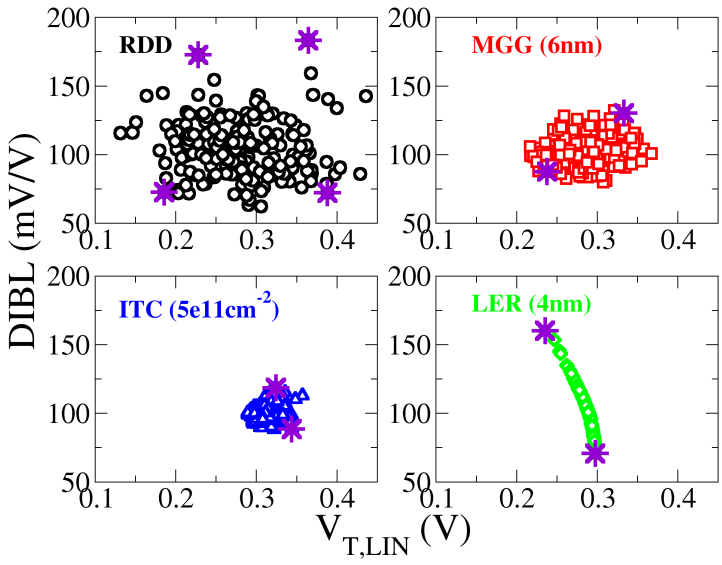


Figure 11. The scatter plot of DIBL with linear threshold-voltage. Large de-correlations are observed in the presence of RDD, MGG and ITC respectively. The devices spotted by stars are under particular examination.

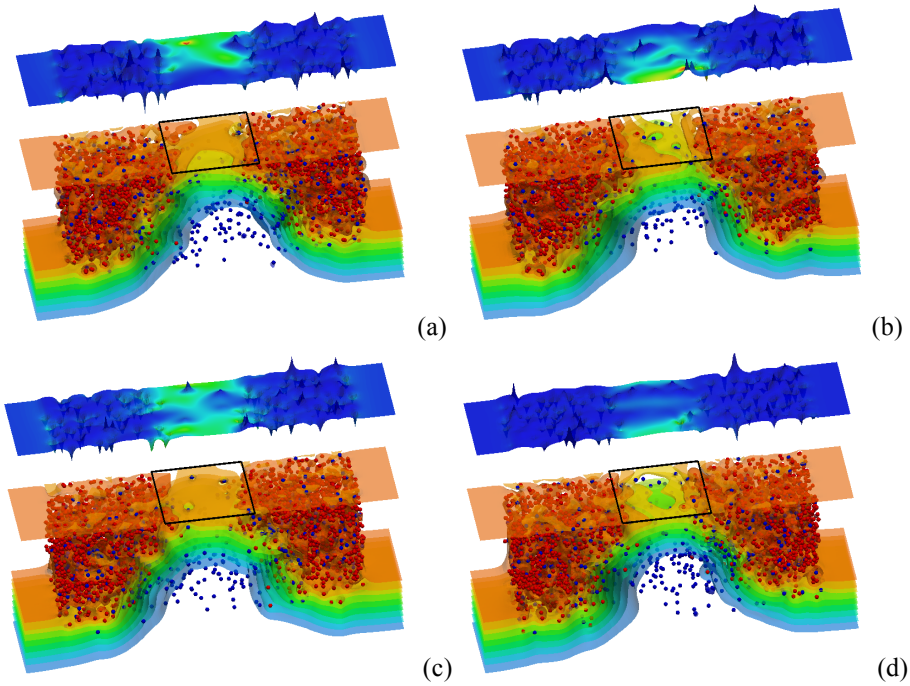


Figure 12. Particular atomistic devices subject to random dopant fluctuation, showing the electron density in the bulk with contours. Blue dots represent ionised acceptors and red dots represents ionised donors. The top slice is the potential landscape close to interface colorised by current density magnitude. The devices are with large DIBL and low $V_T$ (a), large DIBL and high $V_T$ (b), small DIBL and low $V_T$ (c), small DIBL and high $V_T$ (d).

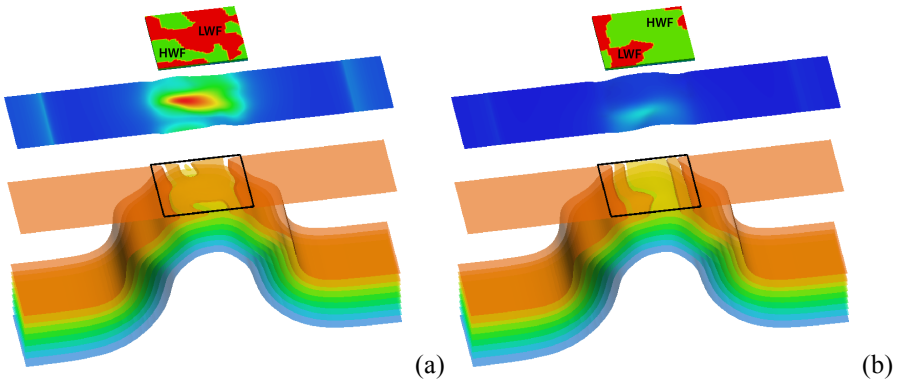


Figure 13. Particular atomistic devices subject to MGG, showing the electron density in the bulk with contours. The slice is the potential landscape close to interface colorised by current density magnitude. The top slab is the potential distribution in the oxide clearly affected by the different effective work functions. The devices are with small DIBL and low $V_T$ (a), large DIBL and high $V_T$ (b).

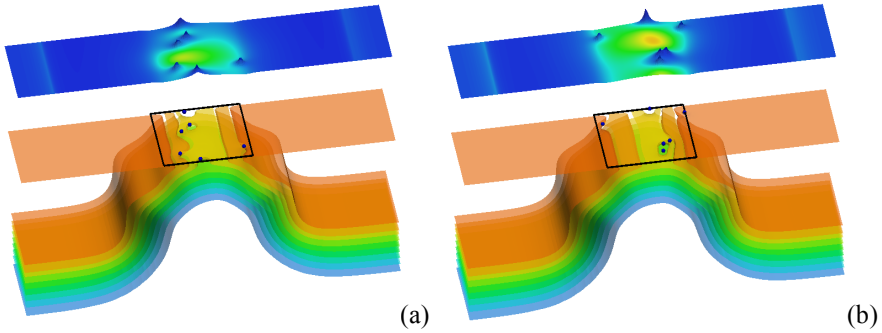


Figure 14. Particular atomistic devices subject to random trapped charges, showing the electron density in the bulk with contours. Blue dots represent the negative charged traps. The top slice is the potential landscape close to interface colorised by current density magnitude. The devices are with the small DIBL (a), large DIBL (b).

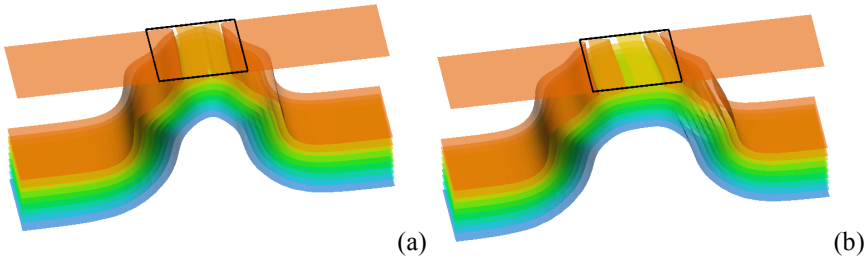


Figure 15. Particular atomistic devices subject to gate LER, showing the electron density in the bulk with contours. The top slice is the potential landscape close to interface colorised by current density magnitude. The devices are with the large DIBL (a), small DIBL (b).

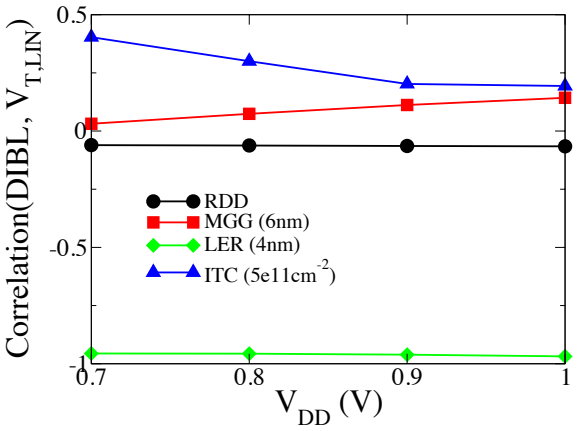


Figure 16. The drain-bias dependence of correlation between DIBL and threshold-voltage.